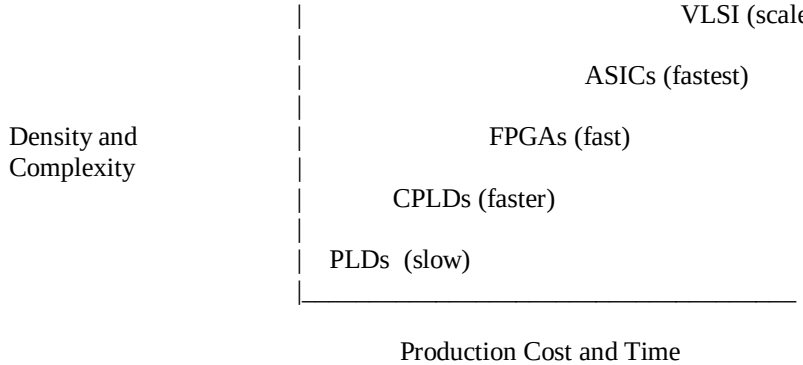
Lecture 8: PLDs and FPGAs

-Traditional IC => Fixed operation defined by manufacturer
-ASIC => User defined manufactured IC (standard cell or gate array)
Have fast clock time because they are completely hardwired
-PLDs => Uses AND gate array with selectable programmable input pins feeding an OR gate as input
Can mimic a state machine by taking the OR gate output as feedback input to the AND gate array
In use for 20 years, completely user programmable
Use 1K to 10K gates
Take 3-10 nsec to produce output and limited by number of input/output pins
Generally use 1 PLD per state machine; each output is a state variable
Limiting factors are # gates or pin resources that are available
Can use PLDs in series, but watch out: 10 nsec delay per PLD!
Can use all kinds of PLDS
-Sequential PLDS for doing sequential circuit function emulation
-Bipolar PLDs for doing basic TTL logic applications (power hog)
-Erasable PLDS using ultraviolet light
-CPLDS => Complex PLDS
Advanced programmable PLDS
Uses a logic "cell" to implement a network of logic gates or flip-flops
Uses 10K to 250K gates!
Have low design utilization due to rigid architecture
Rigid architecture makes them faster than FPGAs
-FPGAs => Large PLD applications: read/write memory used to control logic states
Uses logic "cell" to implement network of logic gates or flip-flops, like CPLDS
Achieves higher utilization of architecture because of higher density of programmable gates
Flexible design allows more programmable routing within the "cell" matrix of gate arrays
Gate arrays broken into logic block sections that communicate via programmable logic
Uses R/W memory to control connection of components
Combines uprocessor and RAM/ROM with ASICs in mind, and useful for PLDs to VLSIs
Have 3 kinds:
Computational logic array – reprogrammable algorithms implemented at gate level (ex. Algotronix CAL1024).
Structured PAL – programmable array logic that uses VLSI functionality of interconnections to create a general purpose device (ex. Altera EP1810).
Channeled FPGA – ASIC like device with field programmable structure in mind. (ex. Xilinix 3000 series). Uses combination of wires, switching matrix and gate logic.



VHDL => Models circuit design that convert PLDs and ASIC gates into a set of primitives (components)
User supplies inputs to target assembly board and the code generates output states of the design
Can add circuit intrinsic time delays to design
Designs are decomposed hierarchically
Logic components have defined interface and operation
Architecture declaration that describes operation/algorithm/function of components
Entity declaration describes the interface of components
Timing and concurrency of operations can be described synchronously or asynchronously