Lecture 5: Digital Design Issues

External event (interrupting) issues:

- -reflections
- -shorts
- -bad connections
- -spurious (edge) events
- -event rate
- -logic gating requirements
- -leakage current
- -ground loops
- -clock duty cycle
- -ISR re-entrant quality
- -need for NMI
- -interrupt priorities
- -missed interrupts
- -ISR usage of global/static variables
- -memory corruption
- -priority inheritance with shared resources

Real-Time monitoring devices

- -software monitor to breakpoint or step through code
  - -problems: requires target memory, I/O port, CPU time, RAM resident code
- -onchip background debugger program which works similar to a software monitor
  - -problems: same as software monitor problems except for CPU time
- -incircuit emulator (ICE)
  - -VxWorks uses product called Tornado
  - -maps resources from target to host
  - -run/test without target hardware
  - -debugs likes a software monitor
  - -offers program traceability and memory examination
  - -problems: expensive, real-time simulation limitations

Other devices to use: logic analyzer, ROM emulator, CAD machine.
To do fast circuitry simulations, you need Programmable Logic Devices (PLDs) or Field Programmable Gate Arrays (FPGAs). Together these items provide fast digital design I/O applications to/from CPU, and can be used for fast external interrupt processing.

Examples of usage: digital cameras, Fourier analysis, noise reduction filters, waveform generators, mathematic modeling tools, run-time reconfiguration tools, real-time controls of digital circuitry.

Moore's Law: the number of transistors per square inch in an IC doubles each year (Gordon Moore, 1965)
Actually: it doubles every 18 months

Digital design considerations:

- -document specifications
- -analog data not necessary
- -sequential circuits depend on previous and present inputs
- -verification of memory contents via checksuming
- -speed of light is limiting factor!!!
  - -why: transistors switch at 10psec rates, but light (3*10**8 m/s) traverses ½" of silicon in only 42psec
- -transistors take ~1/2 nsec to analyze input data to produce output
- -clock duty cycle (clock also needs instructions to tick)
- -cache needed (today are 512 KB, first caches used in 1987 were 1KB)
- -parallel vs serial lines (serial lines don't need sync. clock, slower, can go longer distances)

Processor types:

- 8 bit accumulators – has index register, program ctr, stack ptr, 256 bit resolution (Z80, MC6800)
- CISC – complex instruction set, 100Mhz, 32 bit address bus, up to 64 bit data bus, need less code
- RISC – reduced instruction set, twice as fast (20% of instruction set does 80% of code execution)
- DSP – 1 GHz, almost 100% instru/clock cycle vs 10-20% (instructions pipelined along data bus)
- Note: high instru/clk in CISC/RISC has been achieved with advent of Pentium/I486/68040 procs