

Real-Time Systems ECSE 421
Assignment 10: exam

1) The following tasks are scheduled by the ukernel scheduler task (units are clock ticks):

Task	execution time	period	deadline
T1	2	10	10
T2	2	10	10
T3	10	40	40
T4	10	40	40.

T3 and T4 are delayed by one time unit every time there is a context switch from T1 or T2. Is it possible to make this set of tasks R-M schedulable? Show a Gantt chart over 1 major cycle period.

2) Explain why the tasks in question 1 are necessarily D-M schedulable but are not necessarily R-M schedulable.

The following tasks are scheduled by the ukernel scheduler task (units are clock ticks) for questions 3-5; show the Gantt charts over 1 major cycle period in each question.

Task	execution time	period	deadline
T1	2	10	6
T2	5	10	10
T3	6	20	15.

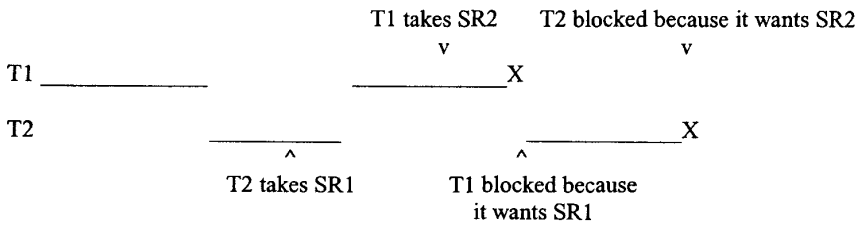
3) Does Earliest-Deadline-First scheduling work for these 3 tasks?

4) Does Shortest-Completion-Time scheduling work for these 3 tasks?

5) Does Least-Slack-Time scheduling work for these 3 tasks?

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For Questions 6 and 7, priorities for tasks T1 and T2 are $P_{T1} > P_{T2}$ for the following timing diagram: T1 and T2 make use of shared resources SR1 and SR2.



6) Explain why Priority Ceiling Protocol solves the above situation whereas Priority Inheritance Protocol does not.

7) If Priority Ceiling Protocol is applied in question 6, does priority inversion still occur? Why?

8) The following tasks are scheduled by the ukernel scheduler task (units are clock ticks).

Task	execution time	period	deadline	priority
T1	2	5	5	1
T2	6	20	20	2
T3	10	40	40	3.

What is task T3's response time per period under Round-Robin scheduling?

What about R-M scheduling? Hint: It may be helpful to sketch the Gantt charts.

9) Every interrupt that comes into your embedded system adds 1 ns to the normal execution time of a task. If two preemptable interrupts are being used, one which is occurring 1% of the time and the other 2% of the time, what is the task's running time (t') in the presence of these interrupts in terms of its normal running time (t) when no interrupts are present?

10) If the two interrupts in question 9 masked each other instead when active, what change (if any) would there be to the answer in question 9?